

IN THE CLAIMS

Please amend the claims as follows:

1-5. (Cancelled)

6. (Currently Amended) A PCI local bus compliant device comprising:

a hardware implemented capabilities list capable of being modified by low-level software, and read-only to higher level software, wherein a modification to the capabilities list by the low-level software modifies capabilities available from the PCI local bus compliant device, wherein the hardware implemented capabilities list comprises a plurality of list nodes that each include a writeable next node pointer register; and

a control register coupled to the writeable next node pointer registers, the control register being operable to change the writeable next node pointer registers to read-only next node pointer registers.

7 - 8. (Cancelled)

9. (Original) The PCI local bus compliant device of claim 6 wherein the hardware implemented capabilities list is writeable by basic input output software and read-only to operating system software.

10. (Original) The PCI local bus compliant device of claim 6 wherein the PCI local bus compliant device comprises an integrated circuit that includes the hardware implemented capabilities list.

11. (Previously Presented) An integrated circuit comprising:
- an address bus;
 - a data bus;
 - a control bus;
 - a series of linked list registers coupled to the address, data, and control busses, the series of linked list registers arranged in a writeable linked list;
 - a control register operable to lock the writeable linked list and conditionally make the series of linked list registers read-only;
 - wherein the control register is writable only by a first level of software and the series of linked list registers are accessible by a second level of software; and
 - wherein the series of linked list registers are arranged in groups, each group forming a linked list node, each linked list node including one next node pointer register.
12. (Cancelled)
13. (Previously Presented) The integrated circuit of claim 11 wherein the control register is operable to make the next node pointer register of each linked list node read-only.
14. (Previously Presented) The integrated circuit of claim 15 wherein the control register is accessible by a first level of software and the series of linked list registers are accessible by a second level of software.

15. (Previously Presented) An integrated circuit comprising:

an address bus;

a data bus;

a control bus;

a series of linked list registers coupled to the address, data, and control busses, the series of linked list registers arranged in a writeable linked list, wherein the series of link list registers include data representative of one or more capabilities of a PCI compliant computer peripheral; and

a control register operable to lock the writeable linked list and conditionally make the series of linked list registers read-only, wherein the integrated circuit comprises a PCI local bus compliant computer peripheral.

16-26. (Cancelled)

27. (Previously Presented) An integrated circuit comprising:

a plurality of register groups, each register group including registers operable to indicate capabilities of the integrated circuit, and including a next group register to point to a next group, wherein the register groups can be written to modify one or more capabilities of the integrated circuit; and

a control register operable to render the plurality of register groups read-only,

wherein the control register comprises a write-once lock bit, that when written, renders the plurality of register groups read-only and the write-once lock bit is configured such that the write-once lock bit can be written to only once between hardware reset sequences.

28. (Original) The integrated circuit of claim 27 wherein the plurality of register groups form a PCI local bus compliant capabilities list.

29. (Original) The integrated circuit of claim 27 wherein the control register is modifiable once by basic input output software, and is not modifiable by operating system software.

30 - 36. (Cancelled)

37. (Previously Presented) A computer system comprising:

a PCI local bus compliant peripheral device coupled to a bus; and
a processor coupled to the bus;

wherein the PCI local bus compliant peripheral device includes a capabilities linked list modifiable by the processor, and wherein the PCI local bus compliant peripheral device further includes a writeable control register operable to render the capabilities linked list read-only by the processor; and

wherein the capabilities linked list comprises a plurality of nodes made up of groups of registers, each node corresponding to one capability and including one writeable next node pointer register.

38. (Cancelled)

39. (Currently Amended) The computer system of claim ~~39~~ 37 wherein the writeable control register is operable to render the writeable next node pointer registers read-only.

40. (Original) The computer system of claim 37 further including a memory device having processor instructions stored therein, the processor instructions being operable to cause the processor to write to the writeable control register.

41. (Original) The computer system of claim 37 wherein the PCI local bus compliant peripheral device includes a writeable register to indicate whether the capabilities linked list is enabled.

42 - 46. (Cancelled)

47. (Previously Presented) A method of initializing a computer peripheral comprising:
 writing a list of capabilities to nodes in a hardware linked list within the computer peripheral during initialization of the computer peripheral; and
 writing to a control register within the computer peripheral to make the nodes read-only.
48. (Original) The method of claim 47 wherein the nodes each include a capability register and a next node pointer register, and writing a list of capabilities comprises modifying the next node pointer register.
49. (Original) The method of claim 47 wherein writing to a control register comprises writing once to a capabilities lock bit, which thereafter is read-only.
50. (Original) The method of claim 47 further comprising writing to a capabilities list enabled register to signify whether the list of capabilities is enabled.
51. (Original) The method of claim 47 wherein the method is performed by basic input output software prior to loading of an operating system.
52. (Original) A method of initializing a PCI local bus compliant device comprising:
 reading instructions from a memory device holding basic input output software;
 modifying a link within a capabilities linked list in the PCI local bus compliant device;
and
 writing to a control register in the PCI local bus compliant device to make the link read-only.
53. (Original) The method of claim 52 wherein the capabilities linked list comprises a plurality of nodes, each node including a capabilities register and a next node pointer register, and wherein modifying a link comprises writing to the next node pointer register.

54. (Original) The method of claim 52 further comprising writing to a capabilities list enabled register.

55. (Original) The method of claim 52 further comprising writing to a head pointer register.

56. (Original) An apparatus having a computer readable medium with machine-readable instructions for a method stored thereon, the method comprising:

modifying a next node pointer register in a PCI local bus peripheral to indicate the existence of a capability; and

modifying a control register in the PCI local bus peripheral to make the next node pointer register read-only.

57. (Original) The apparatus of claim 56 wherein the method further comprises modifying a head pointer register to point to a hardware capabilities linked list, wherein the head pointer register becomes read-only responsive to the control register.

58. (Original) The apparatus of claim 56 wherein the apparatus comprises a read-only memory.

59. (Original) The apparatus of claim 56 wherein the method further comprises modifying a capabilities list enabled register, wherein the capabilities list enabled register becomes read-only responsive to the control register.